ABSTRACT OF THE DISCLOSURE

A non-volatile memory IGFET device has a gate dielectric stack that is di lectrically equivalent ~~in thickness~~ to 170Å or less ~~of silicon dioxide~~. Above the dielectric stack is a polycrystalline silicon gate that is doped in an opposite manner to that of the source and drain ~~junctions~~ regions of the transistor. By using a gate doping that is opposite to that of the IGFET source and drain ~~junctions~~ regions, the poly depletion layer that can occur during programming in modern and advanced memory devices is eliminated according to this invention. The device of this invention forms an accumulation layer in the poly rather than a depletion layer. This difference not only greatly improves the program speed, but allows for selecting the gate doping at levels as low as $10^{11}/cm^3$, or less, without significantly compromising the program speed. Further, since the majority of the applied voltage in a device according to this invention is dropped over the gate dielectric, rather than shared between the gate dielectric and a depletion layer in the gate poly, the device of this invention can be scaled in gate dielectric thickness without significantly compromising the program speed.